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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,160	10/04/2000	James Daniel Merchant	CYPR-CD00055.US.P	1666

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EXAMINER
HAMILTON, MONPLAISIR G

ART UNIT	PAPER NUMBER
2172	

DATE MAILED: 09/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/684,160	Applicant(s) MERCHANT ET AL.	
	Examiner Monplaisir G Hamilton	Art Unit 2172	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "235" (page 10, line 16) "C cell" (page 16, line 17). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to because "2D" should be "3D" (page 24, line 20); "abbreviations... defined, Figure 4" (page 29, line 23) no abbreviations are shown. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
Note: Notice of Draftsperson's Review attached (PTO -948).

Claim Objections

2. Claims 5 and 17 are objected to because of the following informalities: the recitation of a "step e" was disclosed in Claim 4 and 20. Applicant is advised to rename the step. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 5946219 issued to Mason et al, herein referred to as Mason.

Referring to Claims 1 and 14:

Mason discloses a method for configuring a programmable array of logic cells (col 1, lines 5-7). Mason further discloses the use of a CAD tool to facilitate the design process (col 2, lines 45-47). A design database is generated based on the information gathered from a schematic produced by the CAD tool (col 2, lines 52-55). Mason further discloses that elements in the logic design are identified by an instance name (col 2, lines 20-25). The design database disclosed by Mason specifies the logic cells, I/O blocks, and interconnects of the FPGA which will participate in the implementation of the logic circuit, including locations of selected resources and their routing or logic configurations (col 2, lines 55-57). From the configuration information contained in the design database a configuration bitstream is generated by a tool commonly referred to as a bitstream compiler (col 2, lines 65-67).

Mason does not expressly disclose the claimed "a) identifying a plurality of memory cells in a hierarchical schematic representation of said programmable device; b) automatically determining a plurality of addresses corresponding to said plurality of memory cells; c) automatically determining a plurality of logical names for said plurality of memory cells; and d) based on an order in which said plurality of addresses are to be loaded into said programmable

device, automatically storing said plurality of logical names for said plurality of memory cells within a data structure within computer readable memory."

However, the functionality of the method disclosed by Mason is essentially the same as the claimed limitation (col 6, lines 25-35).

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claims 2 and 15:

Mason discloses the limitations as discussed in Claims 1 and 14 above. Mason further discloses that the design database lists each of the instance names of the bits comprising the coefficients C_0-C_7, the locations of their corresponding logic cells (col 7, lines 15-20, 35-40).

Mason does not expressly disclose the claimed "identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy."

However, the functionality of the method disclosed by Mason is essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claims 3 and 16:

Mason discloses the limitations as discussed in Claims 1 and 14 above. Mason further discloses that a coordinate system used to identify the location of logic cells (60, 65), the system disclosed is similar to the Cartesian system.

Mason does not expressly disclose the claimed "b1) determining a wordline associated with one memory cell of said plurality of memory cells; and b2) determining a bitline associated with said one memory cell of said plurality of memory cells."

However, the limitation disclosed by Mason can be used to come up with the claimed limitation. A transformation can be applied to the (X, Y) system as disclosed by Mason to come up with the claimed bitline, wordline system. Therefore, the limitations are essentially the same.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claims 4 and 20:

Mason discloses the limitations as discussed in Claims 1 and 14 above. Mason further discloses that the compiler takes the location and configuration information in the design database and creates the defining bitstrings, which will configure the various resources within the FPGA (col 3, lines 1-5).

Mason does not expressly disclose the claimed" e) repeating said steps a) through d) for each configuration block of said programmable device."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claims 5 and 17:

Mason discloses the limitations as discussed in Claims 1 and 14 above. Mason further discloses that the design database specifies the components that will participate in the implementation of the logic circuit (col 2, lines 54-57).

Mason does not expressly disclose the claimed " determining whether there is a configuration bit at said address in said configuration block."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claims 6 and 18:

Mason discloses the limitations as discussed in Claims 5 and 17 above. Mason further discloses that the design database specifies the components that will participate in the implementation of the logic circuit (col 2, lines 54-57).

Mason does not expressly disclose the claimed "f) placing a spacer in said data structure of said plurality of logical names in said step d) responsive to a determination of step e) that there was no configuration bit at said address in said configuration block."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claims 7 and 19:

Mason discloses the limitations as discussed in Claims 1 and 14 above. Mason further discloses that his invention relates generally to programmable logic devices, and more particularly to the configuration of field programmable gate arrays (col 1, lines 5-10).

Mason does not expressly disclose the claimed" programmable device is a complex programmable logic device (CPLD)."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 8:

Mason discloses a method for configuring a programmable array of logic cells (col 1, lines 5-7). Mason further discloses that the GUI reads in the design database and displays portions of the design database selected by the user (col 6, lines 36-40). Mason further discloses that the bitstream compiler takes the configuration information and the location information and uses this information to generate the bitstrings (Fig 8A, 8B).

Mason does not expressly disclose the claimed "a) accessing a data structure comprising a plurality of logical names corresponding to a plurality of addresses; b) accessing a data structure specifying an order in which said plurality of addresses are to be loaded into said programmable logic device; c) ordering said plurality of logical names from step a) based on the order specified in said data structure in step b); and d) storing said ordered plurality of logical names from step c) in a data structure within computer readable memory."

However, the system Mason describes uses a database to store the logical name and address as well as the order information, which specifies exactly how the device is to be loaded. Therefore the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 9:

Mason discloses the limitations as discussed in Claim 8 above. Mason further discloses that the design database can be updated by entering new configuration information. There is a place to enter the new configuration information for a corresponding instance (Fig 8A).

Mason does not expressly disclose the claimed "storing a placeholder in said data structure of said plurality of logical names from step d)."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 10:

Mason discloses the limitations as discussed in Claim 8 above. Mason further discloses that the design database specifies the components that will participate in the implementation of the logic circuit (col 2, lines 54-57).

Mason does not expressly disclose the claimed " determining whether there is a configuration bit at said address in said configuration block."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 11:

Mason discloses the limitations as discussed in Claim 8 above. Mason further discloses a design entry-module, such as a CAD tool, a schematic capture program, or the like is used to create, and to store onto disk the initial design (col 6, lines 25-35). A place-route module takes the schematic and creates a design database. The database identifies the logic cells, I/O blocks and interconnects by their instance names and locations in the FPGA (col 5, lines 13-16).

Mason does not expressly disclose the claimed "identifying a plurality of memory cells in a hierarchical schematic representation of said programmable device; a2) identifying said plurality of addresses corresponding to said plurality of memory cells; and determining said plurality of logical names for said plurality of memory cells."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 12:

Mason discloses the limitations as discussed in Claims 11 above. Mason further discloses each bit is implemented by a logic cell that is configured to output a constant logic level (col 7, lines 36-40).

Mason does not expressly disclose the claimed "plurality of memory cells are configuration bits."

However, the functionality of the method disclosed by Mason is essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 13:

Mason discloses the limitations as discussed in Claims 11 above. Mason further discloses that the design database lists each of the instance names of the bits comprising the coefficients C_0-C_7, the locations of their corresponding logic cells (col 7, lines 15-20, 35-40).

Mason does not expressly disclose the claimed "identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy."

However, the functionality of the method disclosed by Mason is essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 5384275 issued to Sakashita. Sakashita discloses an arranging and wiring step that is similar to ordering function disclosed by the applicant (Fig 9, col 2, lines 60-65).

US Patent 6438738 issued to Elayda. Elayda discloses generating a sequence of directives dependent on the configuration mode (Abstract).

US Patent 5278769 issued to Bair. Bair discloses logic model generation system based on data in a schematic database (Abstract).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monplaisir G Hamilton whose telephone number is 1703-305-5116. The examiner can normally be reached on Monday - Friday (8:00 am - 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y Vu can be reached on 1703-305-4393. The fax phone numbers for the organization where this application or proceeding is assigned are 1703-746-7239 for regular communications and 1703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 1703-305-3900.

Monplaisir Hamilton
September 4, 2002

KIM VU
SUPERVISORY PATENT EXAMINER
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